State-of-the-art **switching chips** are programmable

- Programmable network packet parsing
- Programmable packet modification instructions
- Programming language e.g., **P4**

**Performance**
- Terabits/second (i.e., Billions of packets/second)

**Limitations**
- Simple arithmetic (+,-) /bitwise logic (AND, OR, ...)
- Small memory (10s MBs), small data bus (512B)
- Small number of instructions per packet

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**A neural network on a network switch?**

- Replace heuristic algorithms with specialized versions
  - Packet scheduling
  - Load balancing
  - Queue management

- Computation offloading
  - Pre/Post-processing
  - Informed “next-hop” selection

- Complement lookup tables for (packet) classification
  - White/black lists
  - Multi-stage classification
  - Specialized hash-functions

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**N2Net**

- Regular Neural Networks
  - Multiplications ✗
  - Act. Func., e.g., Sigmoid ✗

- Binary Neural Networks
  - XNOR ✗
  - Popcount, Sign ✗

- With current hardware
  - line rate throughput with 96 (64, 32) neurons, 32b act.
  - 960M forward passes/sec

- Supporting larger networks at line rate:
  - Likely, ~+5% in chip’s cost

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**Check open positions at:**

[neclab.eu/jobs](http://neclab.eu/jobs)